## What is claimed is:

- 1 1. An integrated circuit, comprising:
- 2 a multiplicity of macro-circuits, each macro circuit having the same function;
- a fuse bank containing a multiplicity of fuses, the state of said fuses storing test
- 4 data indicating at least which macro-circuits failed a test; and
- 5 means for preventing utilization of failing macro-circuits during operation of said
- 6 integrated circuit.
- 1 2. The integrated circuit of claim 1, further including means for isolating inputs and
- 2 outputs of said macro-circuit during testing of said macro-circuits and during testing of
- 3 additional circuits of said integrated circuit.
- 1 3. The integrated circuit of claim 1, further including isolation circuits adapted to, during
- 2 testing of said macro-circuits, isolate each macro-circuit from additional circuits of said
- 3 integrated circuit and couple a single macro-circuit into a single scan chain, the output of
- 4 said single scan chain observable at an I/O pad of said integrated circuit.
- 4. The integrated circuit of claim 1, wherein said macro-circuits include logic built-in test
- 2 circuits.

- 5. The integrated circuit of claim 1, wherein said means for preventing includes a shift
- 2 register for reading out the state of said fuses for passing the state of said fuses to a
- 3 control circuit, said control circuit adapted to disable failing macro-circuits directly or
- 4 adapted to disable failing macro-circuits under the direction of an electronic system said
- 5 integrated circuit is electrically connected to.
- 1 6. The integrated circuit of claim 5, further including:
- 2 one or more repairable circuits, said fuse bank further including additional fuses
- 3 for storing repair data for said repairable circuits; and
- 4 an additional shift register serially connected to said shift register, said additional
- 5 shift register for reading out the state of said additional fuses and for passing the state of
- 6 said fuses to a repair circuit, said repair circuit adapted to replace failing portions of said
- 7 repairable circuits with redundant good circuits.
- 7. The integrated circuit of claim 1, wherein said macro-circuits are microprocessors and
- 2 said means for preventing generates a busy signal for each macro-circuit that failed said
- 3 test.
- 8. The integrated circuit of claim 1, wherein said fuse bank stores compressed data and
- 2 further including means for decompressing said compressed data.

- 9. The integrated circuit of claim 1, wherein said fuses are selected from the group
- 2 consisting of laser blow fuses, electrical blow fuses or electrical blow antifuses.

- 1 10. A method of generating a partial good integrated circuit, the method comprising:
- 2 providing an integrated circuit having a multiplicity of macro-circuits arranged in
- 3 one or more groups, each macro circuit of the same group having the same function, and a
- 4 fuse bank containing fuses;
- 5 isolating said macro-circuits from other circuits of said integrated circuit;
- 6 testing each macro-circuit prior to a fuse programming operation;
- 7 programming said fuses in said fuse bank in order to store data indicating at least
- 8 which macro-circuits failed said testing step; and
- 9 preventing utilization of each failing macro-circuit during operation of said
- integrated circuit based on the data stored in said fuse bank.
- 11 11. The method of claim 10, wherein:
- said integrated circuit further includes first scan chains coupling said other
- circuits, second scan chains coupled to said macro-circuits and isolation circuits coupled
- 14 to third scan chains, said isolation circuits coupled between said other circuits and said
- 15 macro-circuits; and
- further including the steps of coupling said first, second and third scan chains into
- a first configuration to achieve isolation of said other circuits from said macro-circuits
- and coupling said first, second and third scan chains into a second configuration to
- achieve isolation of said macro-circuits from each other and from said other circuits.

- 1 12. The method of claim 10, wherein said testing includes applying sequentially one or
- 2 more test patterns to each macro-circuit in each group macro-circuits and determining
- 3 failing macro-circuits one group at a time.
- 1 13. The method of claim 10, further including keeping a count of failing macro-circuits
- 2 during testing and terminating testing when the number of failing macro-circuits exceeds
- 3 a predetermined number.
- 1 14. The method of claim 10, further including:
- writing data indicating at least which macro-circuits failed to a fuse blow file in a
- 3 tester performing said testing; and
- 4 wherein said programming is performed based on data in said fuse blow file.
- 1 15. The method of claim 10, further including:
- 2 performing a post fuse blow test, said post fuse blow test including in the order
- 3 recited:
- 4 masking each failing macro-circuit based on the data in said fuse bank;
- 5 applying sequentially one or more test patterns to each macro-circuit in
- 6 each group of macro-circuits and determining failing macro-circuits one group at
- 7 a time; and
- 8 terminating post fuse blow test upon any macro-circuit failing.

- 1 16. The method of claim 15, further including in the order recited:
- 2 after performing said post fuse test, packaging said integrated circuit into a
- 3 module; and
- 4 performing a module test, said module test including in the order recited:
- 5 masking each failing macro-circuit based on the data in said fuse bank;
- 6 applying sequentially one or more test patterns to each macro-circuit in
- 7 each group of macro-circuits and determining failing macro-circuits one group at
- 8 a time; and
- 9 terminating module test upon any macro-circuit failing.
- 1 17. The method of claim 10, wherein said macro-circuits are microprocessors.
- 1 18. The method of claim 10, wherein the step of preventing includes generating a busy
- 2 signal for each macro-circuit that failed said test.
- 1 19. The method of claim 10, wherein the step of preventing includes disabling failing
- 2 macro-circuits under the direction of an electronic system said integrated circuit is
- 3 electrically connected to.

20. The method of claim 10, wherein said fuses are selected from the group consisting of
laser blow fuses, electrical blow fuses or electrical blow antifuses.